13.2 An MLSE Receiver for Electronic-Dispersion Compensation of OC-192 Fiber Links

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Electronic-dispersion compensation (EDC) techniques are being explored in OC-192 metro and long-haul links to combat dispersion/intersymbol interference (chromatic and polarization mode), noise (optical and electrical), and non-linearities (fiber, photodiode, laser). In this paper, a 9.953 to 12.5Gb/s MLSE receiver, as shown in Fig. 13.2.1, is presented. The receiver is implemented via an AFE IC and a digital equalizer IC that are packaged in a 23×17mm^2 261-pin MCM. The AFE IC is implemented in a 0.18µm 3.3V GHz SiGe BiCMOS process. The digital IC implements the MLSE algorithm and is fabricated in a 0.13µm 1.2V CMOS process.

The architecture of the AFE IC is shown in Fig. 13.2.2. It features a VGA, a 4b flash ADC, a dispersion-tolerant clock-recovery unit (CRU), and a 1:8 DEMUX. The ac-coupled line-rate input (9.953 to 12.5Gb/s) can be single-ended or differential. The input signal is amplified by the VGA and then sampled by the ADC. The CRU recovers a line-rate clock for the ADC and the DEMUX. The 4b line-rate ADC samples are demultiplexed 1:8 to generate a 32b LVDS interface to the digital chip (see Fig. 13.2.1).

The 3-stage VGA in Fig. 13.2.2 incorporates an analog MUX to achieve a 40dB tunable gain range and an enhanced linearity to meet the requirements of both amplified and un-amplified links. The gain sensitivity to process variations is reduced by employing a replica bias circuit (not shown) to generate source voltage V1 for M1, which is input to the gain-control block, as shown in Fig. 13.2.3. A gain-insensitive offset control maintains a constant offset independent of the input power. Offset control balances the noise variance of '1's and '0's in OSNR-limited links. The need for both single-ended and differential inputs combined with the need for input offset adjustment result in the input-termination scheme in Fig. 13.2.2. A 50Ω input termination is achieved with an S_{11} < -15dB up to 7.5GHz and S_{11} < -10dB up to 20GHz.

The ADC architecture, shown in Fig. 13.2.2, has one stage of pre-amplifiers followed by two stages of metastability FFs (ADC FFs) and a Gray encoder. The Gray encoder limits coding errors to 1 LSB, minimizing their impact on the BER. The ADC can be configured between a 4b and a power-saving 3b mode. The cascode pre-amp reduces VGA output loading. Isolation between the pre-amps, the ADC back-end (ADC FFs and the encoder), and the DEMUX is critical. Guard rings are placed between the pre-amps and the ADC back-end, and between the ADC back-end and the DEMUX. The ground and substrate connections of the pre-amps and the ADC FFs are shared to minimize ground bounce. The DEMUX has its own supply, but it shares the same bias current as the ADC FFs. The swing in the digital blocks is made programmable to strike a balance between substrate injection and noise immunity.

The CRU shown in Fig. 13.2.2 is a bang-bang PLL [1] with a fast differentially tuned VCO and phase filtering that enables clock extraction in the presence of a closed eye. Fiber non-linearities and dispersion spreads the zero crossings and reduces the duty cycle. Conventional bang-bang PLLs generate significant jitter and cycle slips after 70 to 80km of fiber at an OSNR<12dB. The Alexander phase-detector output in Fig. 13.2.2 is filtered to extract phase updates corresponding to low-frequency data patterns. The phase updates have a low- and a high-frequency component, where the latter tracks instantaneous phase changes and only the former is sent off-chip to a loop capacitor using a 4-point tuning-sensing bridge connection. The latter removes inductive peaking caused by the bond wires. The sensing input has a 3rd-order RC π filter to reduce the off-chip noise. The VCO in Fig. 13.2.3 employs a bridge varactor driven by an emitter follower to provide instantaneous frequency updates while increasing common-mode noise immunity. The varactors in the bridge are not identical and are sized to reduce jitter.

The VCO is isolated from hard-switching blocks, such as the clock dividers in the PLL, the ADC FFs, and the DEMUX, in order to reduce noise coupling and avoid injection locking. Blocks in the CRU, VGA, and ADC are matched to provide automatic center-of-eye sampling. The ADC clock and data paths are also matched to provide consistent sampling across all 16 comparators.

The digital IC accepts a line-rate/8 32b LVDS input stream from the AFE IC as shown in Fig. 13.2.1. The 16 parallel 4b data is processed by a 4-state Viterbi equalizer with a look-back of 6 bits. The equalizer determines the most likely path from 2^6 possible paths. State metrics are initialized to zero. The 64 paths are placed into 4 groups of 16 paths each, where each group corresponds to a specific initial state. The path-finder block in Fig. 13.2.1, computes the path metrics in a non-recursive manner until the best path in each group is obtained. The path-selector block employs the past two decisions to select the best overall path from the 4 candidate paths. The best path is used to make a decision on 2 bits. The delayed recursion architecture eliminates the add-compare-select (ACS) recursion and puts a multiplexer chain in the critical path. The path-finder and path-selector architectures are unfolded by a factor of 8 to parallelize the architecture, so that 16b decisions are made in each clock cycle. The channel estimator employs an adaptive Volterra kernel with three linear, three non-linear, and a dc tap. The estimation error is obtained by comparing the ADC output with the Volterra filtered version of the path-selector output. Further details can be obtained from [2].

The two chips are tested independently and together in various fiber plants with a zero-chirp transmitter. Measurement results for the AFE IC are shown in Fig. 13.2.4. The VGA bandwidth is 7.5GHz and linearity is >30dB with a 5GHz two-tone test. The ADC achieves an ENOB=3.5b for data frequency of 5GHz at a sampling frequency of 12.5GS/s. The CRU meets SONET jitter-tolerance specifications [3] with 2200ps/nm of dispersion. The MLSE receiver achieves a BER of 10^{-4} at an OSNR of 14.2dB with 2200ps/nm of dispersion, as shown in Fig. 13.2.5. Other tests show that the receiver provides an error-free (BER < 10^{-15}) post-FEC output, with a pre-FEC BER of 10^{-3} at 10.71Gb/s with 2000ps/nm of dispersion. It exhibits no error-floor down to a BER of 10^{-12} and compensates for more than 100ps of instantaneous differential group delay (DGD) with less than 1.5dB OSNR penalty at BER=10^{-4}. The receiver can track DGD variations up to 30MHz. It consumes 4.5W including the interface.

Figure 13.2.6 summarizes the features of the two-die solution. The chip micrographs are shown in Fig. 13.2.7.

Acknowledgments:
The authors acknowledge the contributions of R. Hegde, J. Janovetz, M. Rowlands, P. Setty, and R. Walker.

References:
[1] R. Walker, Phase-locking in High-Performance Systems, IEEE Press, pp. 34-45, 2003.
[2] R. Hegde, A. Singer, and J. Janovetz, *US Patent Application Publication,* no. US 2004/0264555 A1, Dec., 2004.
[3] Synchronous Optical Network (SONET), GR-253-CORE, Issue 3, 2000.

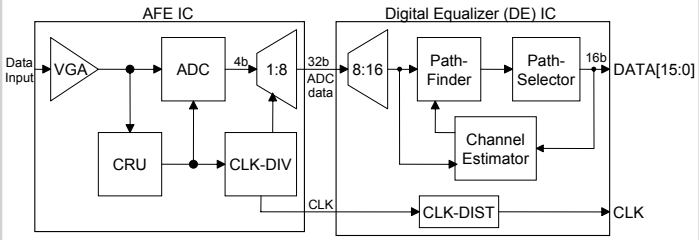


Figure 13.2.1: The MLSE receiver block diagram.

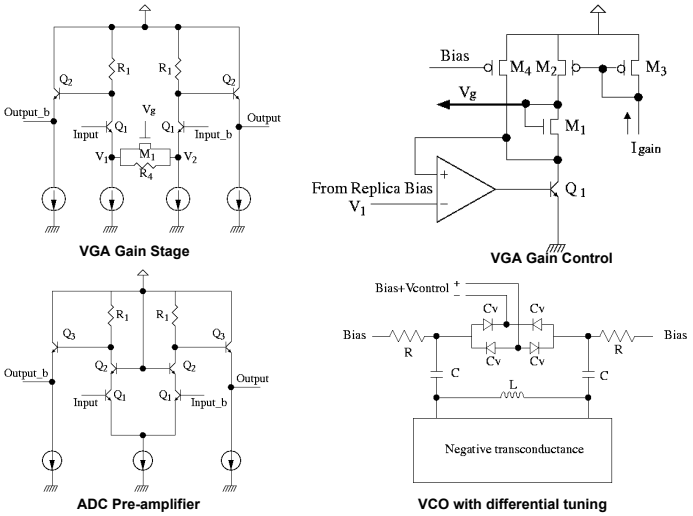


Figure 13.2.3: AFE IC circuit details.

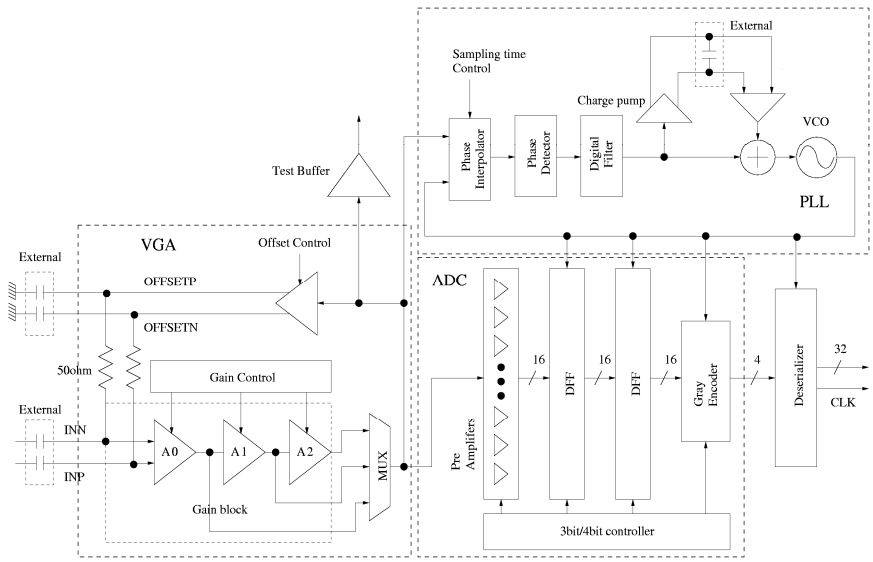
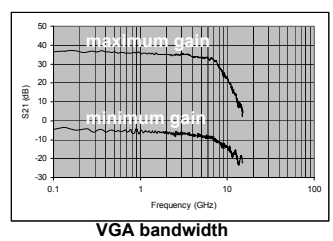
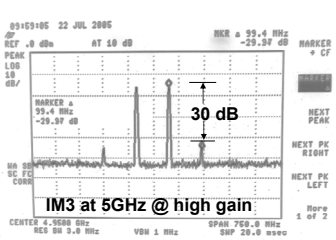
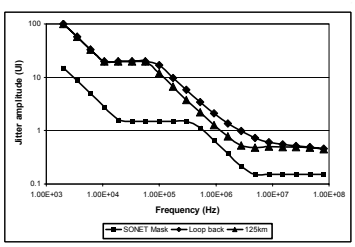


Figure 13.2.2: AFE IC architecture.

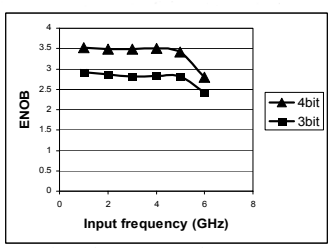


VGA bandwidth





CRU Jitter Tolerance



ADC ENOB with 12.5GHz sampling

Figure 13.2.4: AFE IC measured results.

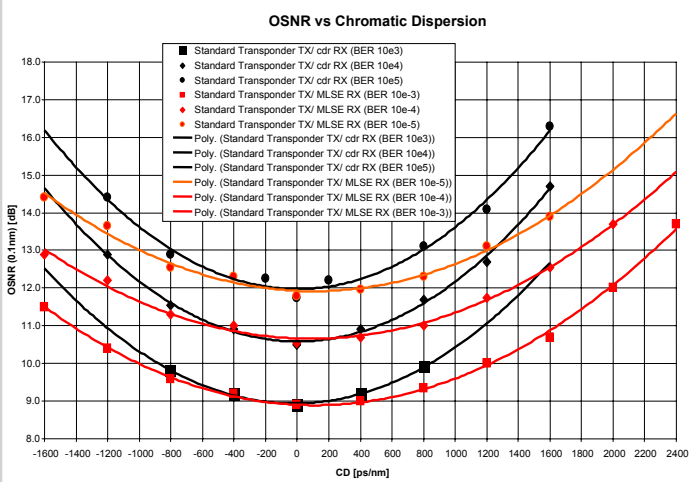


Figure 13.2.5: Measured system test results for the MLSE receiver.

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	Analog Front-End IC	Digital Equalizer IC
Technology	0.18µm SiGe BiCMOS (f_t = 75GHz)	0.13µm CMOS
Supply voltage	3.3V ± 0.3V	1.2V/2.5V (I/O)
Data rate	9.953 to 12.5Gb/s	9.953Gb/s to 12.5Gb/s
Power	3.5W	1.0W
Chip area	25mm^2	25mm^2
# of transistors	34,100=24,900 (FET)+9,200 (NPN)	937,000
ADC ENOB (@ 12.5 GS/s)	>3.4 (4b mode) with 5GHz data	
	>2.8 (3b mode) with 5GHz data	
Output	620 to 781Mb/s LVDS	
Jitter tolerance	meets SONET specs in presence of dispersion	
RX sensitivity	<5 mVppd	
Charge-injection device (CID) tolerence	1300 @ 1E-2 BER, 125km SMF-28	
Packaging	23mm × 17mm, 261 ball FBGA (MCM)	

Figure 13.2.6: Summary of the MLSE receiver.

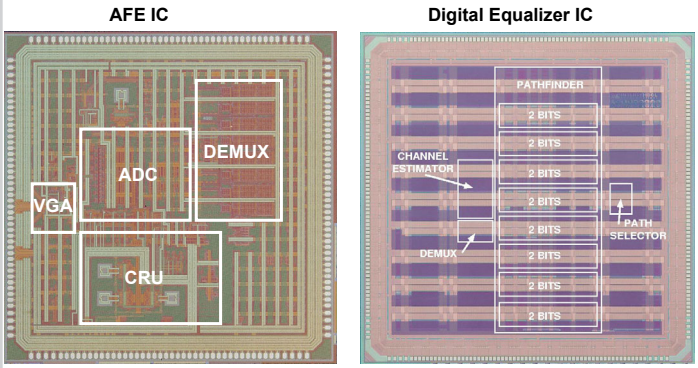

Figure 13.2.7: Chip micrographs.

